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Flip chip electrical interconnection by selective electroplating and bonding

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Abstract This work presents a parallel electrical interconnection process by means of flip-chip, selective electroplating and bonding. The electrical interconnection lines are built on a glass substrate made of 500/2000 Å of Cr/Au with 3150 μm in length and 10 μm in width. Two silicon chips are processed as the device chips to be electrically interconnected. It has been demonstrated that 98 out of 102 interconnects are established in parallel with a successful rate of 96% and the average resistance of the electroplating bond is 12 Ω. This process has potential applications in replacing the conventional, serial wire bonding or tape automated bonding (TAB) process for massive interconnection requirements in IC or MEMS devices. Reliability test is also performed by putting the interconnects into boiling liquid nitrogen (−195 °C) repeatedly. It is found that 100% of the interconnects survive after 2 cycles of the quenching process.

1
Introduction

As demands in miniaturization and functionality increases, high-density interconnection and high-number of I/O requirement are indispensable in the IC and MEMS industry. For example, in the application of focal lens arrays for telescope application [1], millions of micro-mirrors have to be controlled individually and millions of wire bonds have to be established. In some applications, monolithic integration [2–4] of mechanical microstructures and microelectronics is feasible with advantages such as low cost, reduced electrical parasitics and increased operational speed. However, the incompatibility and cross-contamination between CMOS and MEMS fabrication processes often limit such integration processes. Therefore, hybrid integration is currently the major scheme to combine MEMS and IC circuitry and traditional wire bonding [5], tape automated bonding (TAB) [6] and flip-chip [7] have all been demonstrated for integrated microsystems.

Wire bonding has difficulty in achieving high density due to the physical limitations of wire diameter, wire length, and loop height. TAB is not suitable for long-term durability due to the usage of plastic materials. Instead of using conventional wire bonding technology that requires millions of bonding operations or TAB, this work presents a new, one-step approach for high-density electrical interconnection by using flip chip selective electroplating and bonding massively and in parallel.

2
Fabrication process and experimental results

Figure 1 shows the schematic of the new approach. Parallel interconnection is to be established on two separated chips. The interconnection substrate that has patterned metal lines is to be flip chip bonded with the two device chips to establish electrical interconnects. The fabrication process starts with 500/2000 Å Cr/Au deposition and patterning to form bonding pads and interconnection lines in this demonstration example as shown in Fig. 1a. The interconnection chip has 102 Cr/Au interconnection lines with 3150 μm in length and 10 μm in width. The bonding pads on the ends of the interconnection lines are 40 μm by 40 μm. A 0.8 μm thick layer of aluminum is evaporated and patterned as the conducting layer for electroplating on the device chip as shown in Fig. 1b. The wafer is then coated with a 1.1 μm thick photoresist layer and bonding pad areas are opened for electroplating and bonding as shown in Fig. 1c. A spacer layer made of 3 μm thick nickel with an area of $80 \times 80\ \mu m^2$ is selectively deposited as shown in Fig. 1d. This spacer layer increases the space between the interconnection and device substrates to enhance the ion diffusion during the final electroplating and bonding process. The system is now aligned manually by micromanipulators and put into the nickel plating bath as shown in Fig. 1e. The electroplating process is carried out at 50 °C, current density of 22.5 A/m^2 for 80 min. After the

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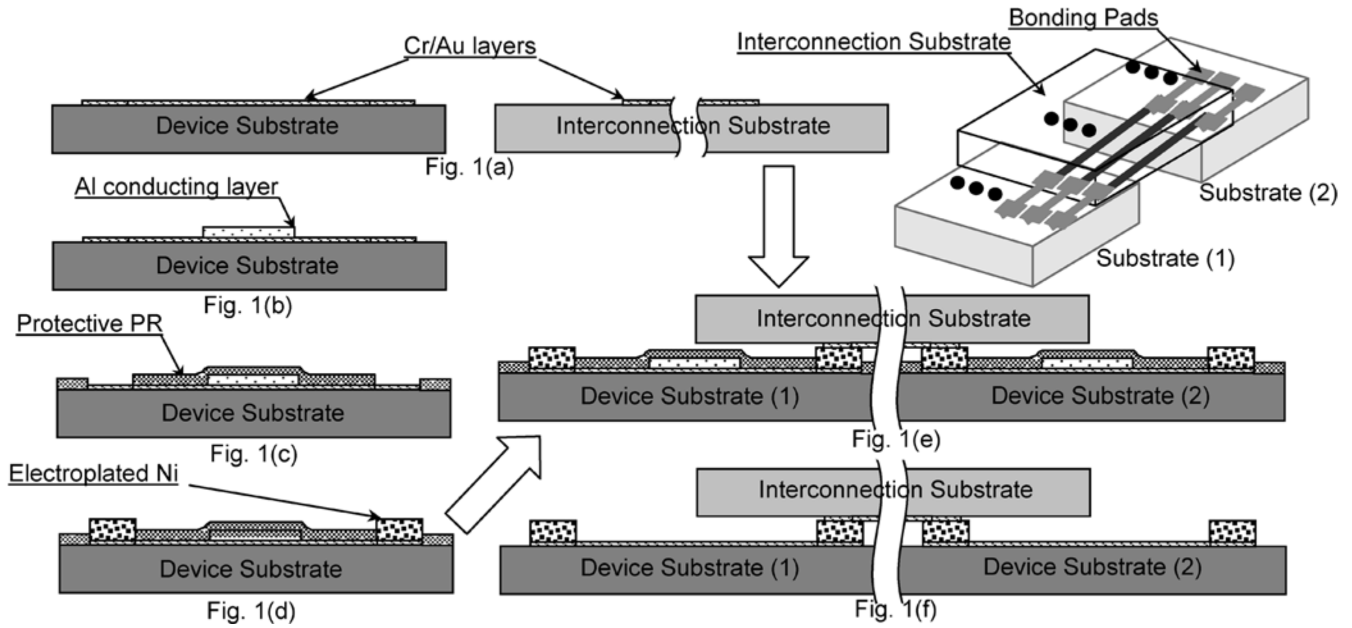

Fig. 1. The fabrication sequence

bonding process, acetone is used to strip off the photoresist and the aluminum layer is removed by diluted HF (1:20) as shown in Fig. 1f.

Figure 2 shows the fabrication result. There are 102 interconnection lines and 98 interconnects are successfully established. The resistance of a single interconnection line after the bonding process is measured as 37 Ω. The measurement of the overall interconnection resistance including the two electroplating bonds is shown in Fig. 3 and the measured average resistance is 62 Ω. Therefore, the average resistance of each electroplating bond is estimated as 12 Ω. The contamination on the bonding surface is the possible reason of the four failed interconnects. Moreover, the accessibility of nickel ions will affect the deposition thickness and quality. For example, for interconnects that are at the edges of the chip are easy to get ion exchange and it is observed in Fig. 3 that their resistance values are generally lower than the average resistance of 62 Ω.

To investigate the thermal cycling effect on the interconnects for possible outer space applications [1], cold quench experiment was conducted by submerging the integrated chips in boiling liquid nitrogen at 1 atm, −195 °C for 2 min. The chips are put in the air for 30 min until room temperature is reached. The resistance of each interconnect is then measured and the cycle is repeated. Figure 4 shows the resistance measurements after the 0, 5th, 10th and 20th cycles.

It is observed that all interconnects keep intact after the first 2 cycles. A total of 12 interconnects break after 5 liquid nitrogen quenches and 56 interconnects break after the 10th quench. The number of broken interconnects saturates after the 10th quench. Resistance fluctuation is observed on interconnects next to the broken ones

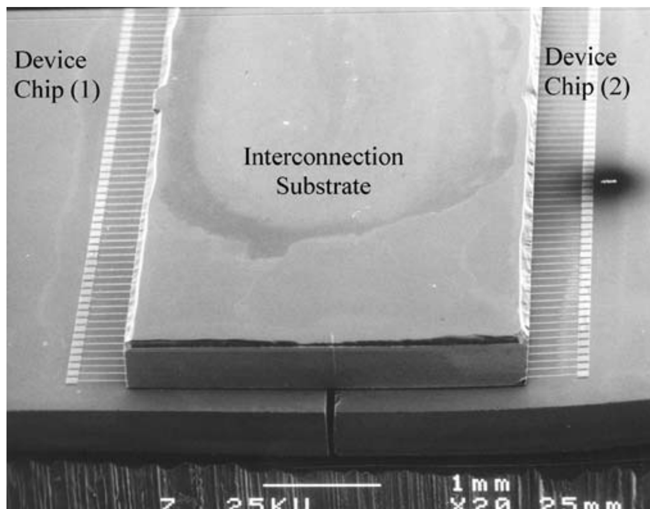

Fig. 2. The fabricated parallel interconnection

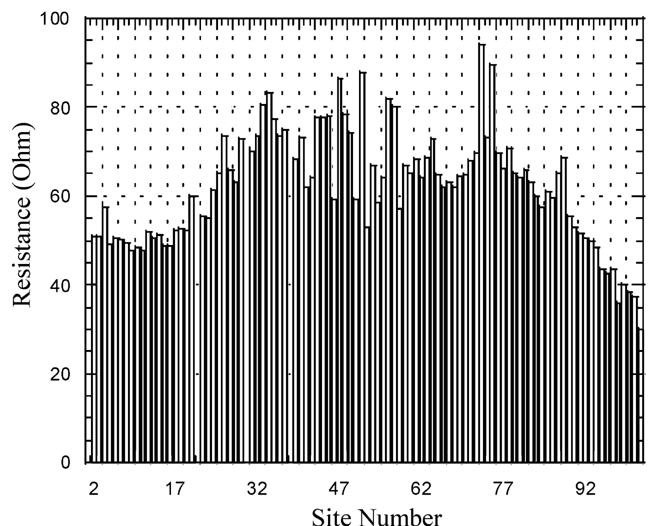

Fig. 3. The resistance measurement of finished interconnections

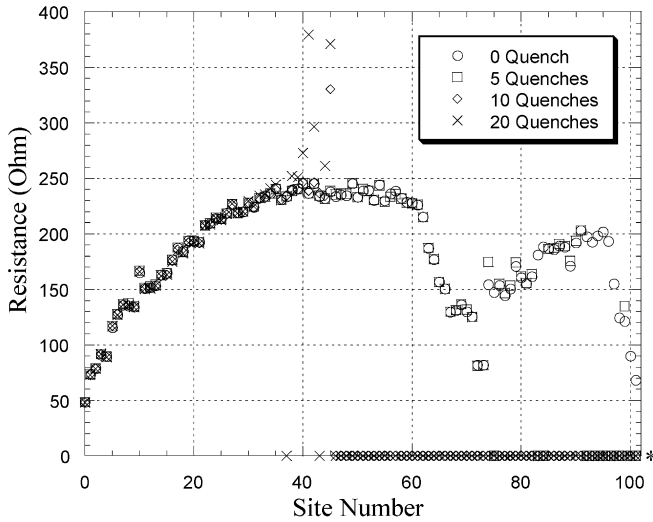

Fig. 4. Resistance measurements after quenching cycles from 25 to −195 °C. *: Zero resistance represents broken interconnects

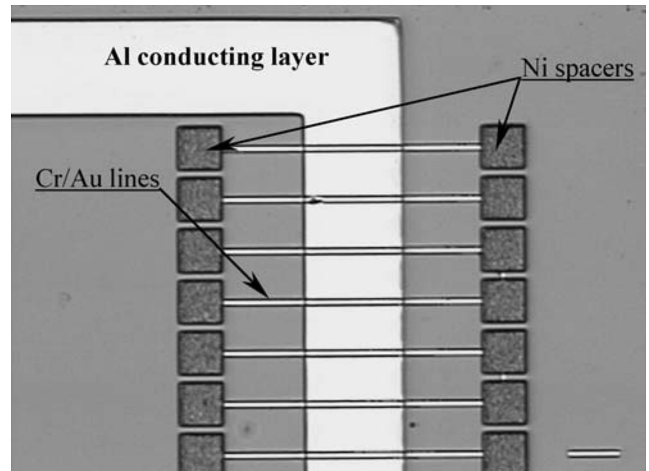

Fig. 6. The optical micrograph of the Al conducting layer and Ni spacer

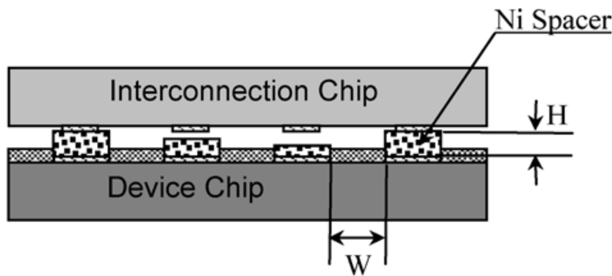

Fig. 5. Various spacer heights due to poor process control

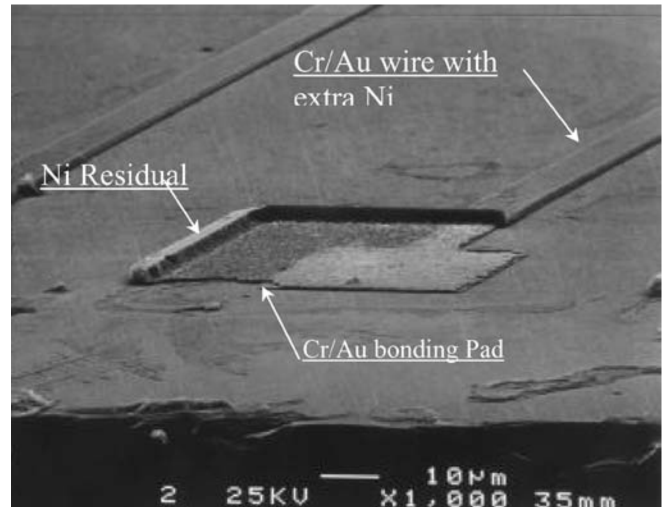

Fig. 7. The SEM microphoto of the interconnection substrate after breaking the bond

possibly due to the stress redistribution from the adjacent broken interconnects. It is found that 43% of the interconnects survive after 20 cycles of the quenching process.

3 Discussions

3.1 Design rules

Electroplating process introduces lateral deposition and proper separation between the adjacent bonding pads is required to avoid short circuit. Figure 5 illustrates the cross sectional view of this situation. In Fig. 5, H represents the distance between the nickel-electroplated spacer and the top interconnection substrate. W represents the separation distance between two bonding pads. The spacers may have various heights due to the poor process control in the electroplating process. Therefore, in order to assure successful bonding results on all interconnects, it is recommended that the electroplating and bonding thickness is H and $W > 2H$ to avoid short circuit. In this work, H is 3 μm and W is 16 μm while the thickness of electroplating bonding process is 3 μm.

An aluminum conducting layer on the device substrate is used to provide uniform current during the electroplating process as shown in Fig. 6. This conducting layer needs to be thick to cover the step created by the Cr/Au lines. To overcome the geometrical shadowing effect between the conducting layer and the Cr/Au lines, a layer of 0.8 μm thick of aluminum is used in this work. On the other hand, the protective photoresist layer as shown in Fig. 1e may block electrolyte transmission. Therefore, spacers with adequate thickness are necessary to provide better ion exchanges to the bonding interface. It is found that electroplated spacer with 3 μm in height is adequate to achieve good bonding results.

Furthermore, when interconnects are created across the two device chips, it is important to level two chips. Otherwise, longer electroplating time is required and the rate of bonding failure may increase.

3.2 Bonding interface

After the bond is forcefully broken, Figs. 7 and 8 show the SEM microphotos of the interconnection substrate and the device chip, respectively. As seen in Fig. 7, the Cr/Au wires on the interconnection substrate have electroplated nickel of about 3 μm because they are not protected by photo-

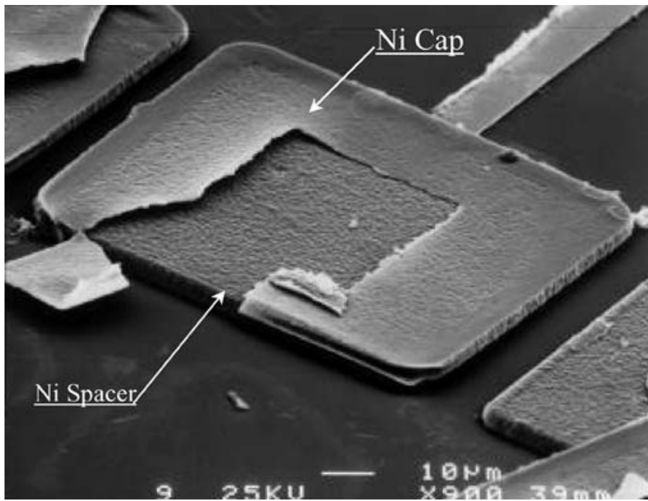

Fig. 8. The SEM microphoto of the spacer after breaking the bond

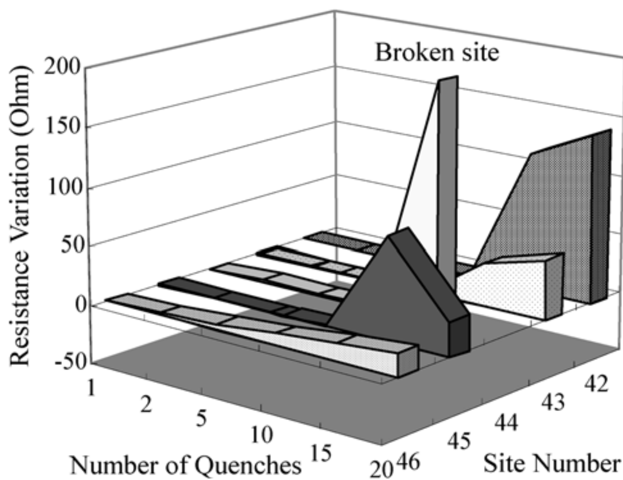

Fig. 9. The resistance variation of interconnects near a broken site

resist during the electroplating process and this extra deposition reduces the resistance of the wire. Furthermore, one may observe a strip of residual nickel that is about 3 μm in width and 3 μm in thickness on the edge of the spacer area and its formation is believed as the result of lateral nickel deposition on the spacer. In the SEM microphoto of Fig. 8, it can be observed that nickel structure on top of the spacer is coarse as compared with the one on the edge of the spacer. This phenomenon is probably due to the fact that ion supply to the interface region between the spacer and the interconnection substrate is limited as compared with the ion supply on the edges of the spacer as shown in Fig. 5. It is also observed that an area of 40×40 μm at the central region (the reflection of the Cr/Au bonding pad on the interconnection substrate) is missing in this interconnect. This shows the bonding strength at this site is weak. The newly grown nickel for bonding is estimated as 0.5 μm in this figure and the majority of them are attached to the nickel spacer.

3.3
Thermal cycles

It is observed from Fig. 4 that interconnects with higher site numbers (higher than 40) tend to break after 10 thermal cycles. One possible reason is that a mechanical clip was placed there in order to fix the interconnection substrate and the device chip during the bonding process and this may create uneven pressure and bending of the substrate locally [8]. After the completion of the bonding process, the mechanical clip is removed but the residual stress is introduced. It is believed that this residual stress plays an important role in the thermal cycling that speeds up the failure process [9]. On the other hand, some of the interconnects exhibit resistance increase before the final failure such as those shown in Fig. 9 of site number 42–46. This behavior may be employed as a diagnosis indicator to the health of interconnects.

4
Conclusions

Flip chip electrical interconnection by selective electroplating and bonding has been successfully demonstrated in this paper. Ninety eight out of 102 interconnects have been accomplished with an average resistance of 62 Ω. The estimated resistance of electroplating bond is 12 Ω for bonding pads of 40×40 μm. A durability test is performed by altering the environmental temperature from 25 to −195 °C. It is found that 48 out of 102 interconnects are functional after 20 thermal cycles. Post-bonding residual stress due to the uneven bonding pressure is believed to accelerate the failure of interconnects such that evenly distributed bonding pressure is suggested for the future improvement.

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