Local synthesis of silicon nanowires and carbon nanotubes on microbridges

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Resistive heating of microline resistors was used to activate vapor-deposition synthesis of silicon nanowires and carbon nanotubes in a room-temperature chamber. The process is compatible with on-chip microelectronics and eliminates the necessity of postsynthesis assembly of nanostructures to form more complicated devices. The process is localized, selective, and scalable. The synthesized nanowire dimensions are 30–80 nm in diameter and up to 10 μm in length, while nanotubes 10–50 nm in diameter and up to 5 μm in length have been demonstrated. Growth rates of up to 1 μm/min for silicon nanowires and up to 0.25 μm/min for carbon nanotubes were observed. This method facilitates the integration of nanotechnology with larger-scale systems. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1587262]

The unique electrical, mechanical and optical properties of nanowires and nanotubes have made them extremely attractive for a variety of applications.[1–6] However, a significant obstacle in the application of these nanostructures has been the difficulty in handling, maneuvering, and integrating them with microelectronics to form a complete system.[2,5–9] Current synthesis processes for silicon nanowires and carbon nanotubes require high temperature furnaces that could damage pre-existing microelectronics. We present an approach that allows the synthesis, in a room temperature chamber, of a desired nanostructure at a prespecified location while eliminating the requirement of later assembly processes. This localized selective synthesis process is capable of direct integration of either silicon nanowires or carbon nanotubes with larger-scale systems, such as foundry-based microelectronics processes. The approach is based on localized resistive heating of suspended microstructures in a room-temperature chamber [Fig. 1(g)] to activate vapor-deposition synthesis and yield either silicon nanowires or carbon nanotubes.

Two types of suspended microelectromechanical systems (MEMS) structures were fabricated to serve as localized microresistive heaters for the synthesis processes: polysilicon microstructures using a standard surface micromachining process[10] and single crystal silicon (SCS) microstructures based on a silicon on insulator (SOI) wafer[11] [Figs. 1(a)–1(f)]. In both cases the microstructures were heavily doped with phosphorus and suspended 2 μm, defined by the sacrificial silicon dioxide layer, above a silicon substrate for electrical and thermal isolation. The typical thickness of the bridges is 2 μm for polysilicon microstructures and 20 μm for SCS microstructures. The wet chemical release etching process naturally creates recessed regions underneath the electrical contacts such that a maskless catalyst deposition process cannot cause an electrical short circuit.

For the silicon nanowires, approximately 5 nm of a 60% gold–40% palladium mixture was sputtered onto the surface to serve as the catalyst.[12] After attachment to a circuit board, the microstructures were placed in the room temperature vacuum chamber. The vapor phase, silane (10% SiH_4–90% Ar), was introduced at 350 mTorr and the microbridge was heated to initiate the silicon nanowire synthesis process. In practice, by applying and steadily incrementing the voltage while recording the current, localized resistive heating of the suspended bridge can be monitored. Figure 2(a) shows the synthesis of silicon nanowires on a 100 μm long, 5 μm wide polysilicon microbridge under localized joule heating for 15 min. They are 30–80 nm in diameter and up to 5 μm in length. The oblique view microphoto of the center region in Fig. 2(b) and the top view microphoto at the edge of the growth region in Fig. 2(c) clearly show location-dependent growth patterns as the result of a nonuniform temperature distribution on the microbridge. We assess the temperature on the microstructures based on the geometry, doping level, and current–voltage

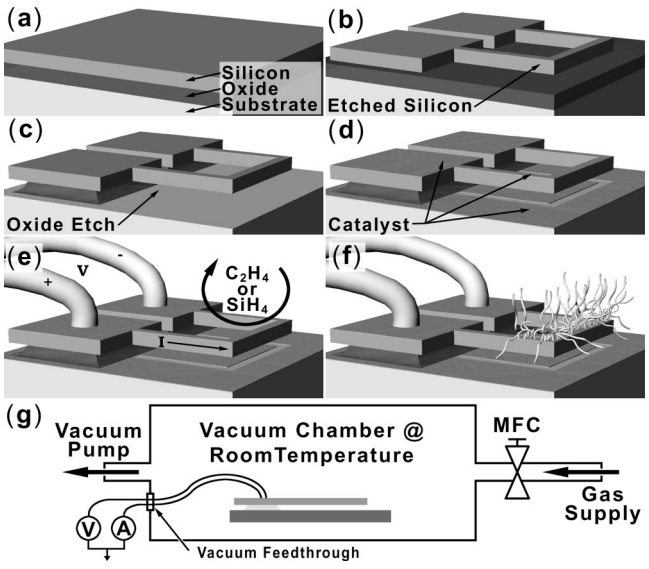

FIG. 1. Series depicting the fabrication of microbridges, growth of nanostructures and experimental setup and process. (a) Initial three-layer wafer. (b) Microstructure layer patterning and etching. (c) Timed etch of the sacrificial oxide layer. (d) Maskless catalyst evaporation. (e) Wirebonds and electrical actuation in the desired gaseous ambient. (f) Resulting nanostructures. (g) Schematic of the experimental setup in a room-temperature chamber.

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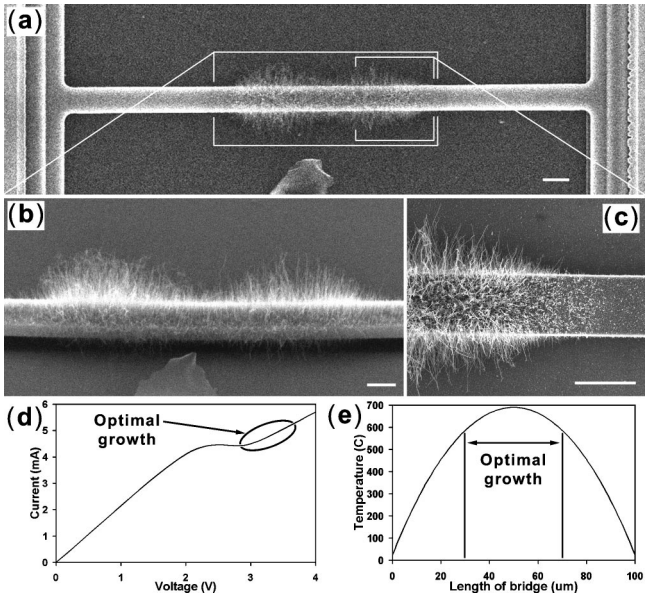

FIG. 2. Localized silicon nanowire growth on a suspended polysilicon microbridge. (a) Silicon nanowire growth region on a 100 μm long and 5 μm wide polysilicon bridge, where the growth region spans approximately 35 μm at the center of the structure. (b) Closeup, oblique view of the nanowire growth region, showing the shorter nanowire region at the center of the structure where the heat dissipation rate is believed to increase due to downward self-buckling of the structure. (c) Top view illustrating the nanowire growth/nongrowth interface indicating the location where the temperature was not sufficiently high to initiate nanowire growth. (d) Experimental current–voltage relationship for the microbridge; nanowire growth took place beyond the linear region. (e) Simulated distribution of the temperature along the surface of the microbridge. The center section, approximately 35 μm long, indicates a sufficiently high temperature for nanowire growth. All scale bars are 5 μm in length.

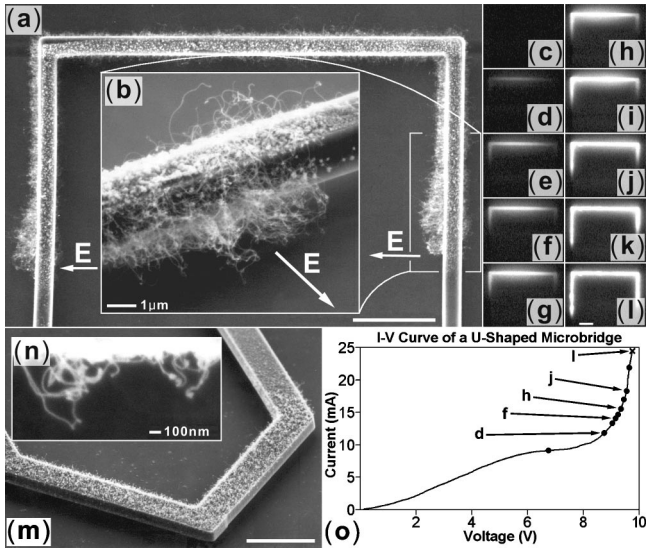

FIG. 3. Nanotube synthesis. (a) Synthesis localized to microbridge legs. Growth occurs largely in the direction of the local E field. (b) High-resolution SEM of the right microbridge section (oblique view). Note how the CNT curves and follows the E field. (c)–(l) Series of optical photographs of microbridge heating. Maximum growth occurs where glow is barely visible, and this corresponds to 850–1000 °C. (m) CNT growth (5 min) localized in the center of a pointed microbridge. (n) High-resolution SEM of a CNT with diameter of ~40 nm. (o) Experimental $I-V$ data from microbridge heating. Data points correspond to (c)–(l). The growth shown in (a) corresponds to the actuation region between point (h) and point (j). All scale bars are 10 μm in length, unless otherwise marked.

characteristics.[13] The experimental current–voltage relationship is shown in Fig. 2(d) and a profile of the temperature of the microbridge is simulated in Fig. 2(e). The current–voltage curve is characteristically linear under low input power and becomes nonlinear when the input power is high due to local high temperatures and secondary effects.[14]

One can conclude that the localized silicon nanowire synthesis process is a strong function of the local temperature, and there appears to be an ideal temperature window at which the reaction takes place. This ''reaction'' is understood to be constituted of a number of processes,[15] all of which depend on the temperature. The thin catalyst layer breaks down into discrete nanoparticles;[12] at the catalyst surface the SiH_4 vapor decomposes into silicon and hydrogen gas, subsequently forming a liquid catalyst-silicon alloy;[16,17] during the synthesis process, the catalyst-silicon alloy continues to absorb silicon until it becomes supersaturated; at the liquid–solid interfaces, silicon then precipitates from the alloy in the form of nanowires.[16,17] It is believed that the microbridge in Fig. 2 has self-buckled downward toward the substrate during synthesis due to compressive stress generated by thermal expansion of the bridge microstructure.[18] As a result, the temperature at the center of the bridge lowered due to better heat dissipation to the substrate, and the nanowires in this area grew more slowly as evidenced in Fig. 2(b). At the growth/nongrowth interface region in Fig. 2(c), breakdown of the thin gold–palladium film into nanoparticles was observed. However, the temperature was not sufficient for the formation of silicon nanowires. An additional advantage of this approach is that a wide temperature distribution from room to high temperature (25–700 °C) can be tested to characterize the growth of nanowires at various temperatures in a single experiment.

For nanotube synthesis, the same method and phenomena are applied. To serve as the catalyst, a 5 nm evaporated nickel, iron, or Ni–Fe (80%/20% by weight) mixture was used, with higher growth rates occurring when iron was present. After placement in the vacuum chamber and being electrically connected, acetylene (C_2H_4) was introduced to supply carbon. With the acetylene pressure constant at 245 mTorr, growth occurred at 0.25 μm/min at optimal temperature locations. Further investigation is ongoing to analyze the dependence of the growth rate on the pressure. Carbon nanotube (CNT) growth requires higher temperatures for the synthesis reaction to occur;[5] higher voltages and currents are therefore required for similar MEMS microstructures.

Figures 3(a) and 3(b) show CNT growth localized mainly to the legs of a ''U-shaped'' microbridge and Figs. 3(c)–3(l) give a series of optical photographs of a similar bridge when electrically actuated. There is a distinct range of temperature at which carbon nanotubes will grow,[5] and this can be used to select the region for synthesis, i.e., in between an area that is too cold (<850 °C for single-walled CNTs) and one that is too hot (>1100 °C). This series shows that the growth region (barely glowing) can be isolated at a desired location on the bridge. Each ''hot spot'' is stationary and stable for a sufficient amount of time to grow nanotubes of at least 5 μm. Figure 3(l) illustrates the bridge just before failure due to melting (~1400 °C).[19] Figure 3(m) displays nanotube growth localized to the center portion of a ''pointed'' microbridge and Fig. 3(n) is an enlarged view of

nanotubes in the center portion of this microbridge. Figure 3(o) gives the electrical characteristics typical of resistive heating of a suspended microbridge. The data points correspond to the photographs in Figs. 3(c)–3(l). The growth shown in Fig. 3(a) occurred between data points (h) and (j) in Fig. 3(o). The nanotubes shown are 10–50 nm in diameter and up to 5 μm in length. It is believed that these nanotubes are multiwalled due to their size and the structural integrity visible in scanning electron microscopy (SEM) microphotos. Carbon nanotube growth response to an applied electric field is well documented;[20] we have also demonstrated the orientation of nanotubes as a function of the electric field applied in Fig. 3(a). The bottom right side of this U-shaped bridge was taken to be approximately 7 V, whereas the bottom left side was grounded. It is seen that the growth direction is fairly well aligned to the electric field. The oblique view in the inset shows the CNT from outside the bridge curving according to the electric field.

It was observed that the microstructures' maximum temperature was not located at the center, but skewed off center by as much as 20% of the bridge length. This was most pronounced in the U-shaped bridges, and the skew was always in the direction of the cathode for both polysilicon and SOI microstructures. This off-center heating, known as the Thomson effect,[21] must be considered when designing the microstructure for localized synthesis. Furthermore, if the microbridges are insufficiently doped, the $I-V$ characteristic is altered dramatically and the temperatures are much less predictable. This can be attributed to secondary effects such as electromigration, grain growth, and localized melting.[21]

In summary, room-temperature synthesis of nanowires and nanotubes in direct contact with MEMS structures was demonstrated. The process yielded localized regions of silicon nanowires, 30–80 nm in diameter and up to 10 μm in length, and carbon nanotubes, 10–50 nm in diameter and up to 5 μm in length. Growth rates of up to 1 μm/min for silicon nanowires and up to 0.25 μm/min for carbon nanotubes were observed. Our process allows direct integration of nanostructures with larger-scale systems and permits the placement of these nanostructures at predetermined, specific locations along the surface of a larger-scale system using the concept of localized heating. This process, therefore, eliminates the need for additional assembly steps and provides a microelectronic compatible technique for the integration of nanotechnology.

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