Room temperature fast synthesis of zinc oxide nanowires by inductive heating

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ZnO nanowires have been rapidly synthesized using inductive heating in a room temperature environment. Nanowires with random and aligned orientations were grown on silicon and 4*H*-SiC (0001) substrates in less than 5 min, respectively, using ZnO/graphite as the solid source powder. Scanning electron microscopy showed nanowire diameters of 20–120 nm and lengths up to 5 μm, and transmission electron microscopy verified the single-crystalline lattice of the nanowires. Electrical properties were studied by connecting a single ZnO nanowire in the field-effect transistor configuration. This demonstration further illustrates the feasibility of a simple and fast nanoscale synthesis using inductive heating for nanomaterial synthesis. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2709618]

One-dimensional (1D) nanostructures such as nanowires and nanotubes have attracted great interest for the past decade because of their specific physical properties and their potential as building blocks for next-generation devices.[1,2] Among them, zinc oxide (ZnO) nanowires have been under intense study for applications as nanolasers, photodetectors, and gas sensors,[3–6] which utilize the unique characteristics of ZnO nanowires including a wide band gap and large surface-to-volume ratios. Furthermore, ZnO nanowires have also been used as field emitters and atomic force microscope tips,[7,8] as they have good hardness, thermal stability, and resistance to oxidation. Therefore, efforts in various synthesis methods have been demonstrated for the growth of high quality 1D ZnO nanostructures, which are very important to the realization of high performance nanoscale devices. Metal organic vapor-phase epitaxy,[9] physical vapor deposition,[10] and aqueous method[11] have been reported in literature for the synthesis of ZnO nanowires/nanorods. However, most methods require very long processing times with low growth rates.

This work presents the inductive heating assisted fast synthesis of ZnO nanowires using ZnO/graphite solid source powder in a room temperature environment. The internal heat generation induced by the alternating magnetic field at the synthesis specimen enables the fast temperature transition for ZnO nanowire growth, with a synthesis time less than 5 min compared to conventional methods. Furthermore, this demonstration illustrates the feasibility of a simple and fast nanoscale synthesis using inductive heating[12] for nanomaterial synthesis.

Figure 1(a) shows the schematic illustration for the ZnO nanowire synthesis setup. The synthesis specimen is placed inside a quartz tube underneath the center of an eight-turn inductive coil with a pitch of 3.25 mm and an inner/outer diameter of 12.7/19.2 mm. The distance between the coil base and the synthesis specimen is ~6 mm. The cross sectional view of the synthesis specimen, including a nickel-coated heating chip, source powder, and growth chip inside a ceramic boat, is shown in Fig. 1(b). When an alternating current is applied in the coil, an alternating magnetic field is generated, which induces eddy currents in the nickel layer and provides rapid Joule heating for nanowire synthesis. Analytically, one can derive each coil's magnetic field intensity generated at any point with a scalar distance of d with respect to the coil loop center from Biot-Savart's law

$$H_{(d.\theta)} = \frac{Ir}{2(r^2 + d^2 - 2rd\sin\theta)}, \quad (1)$$

where I is the current in the coil loop, r is the average radius of the coil, and θ is the angle between the vector of $\vec{d}$ and the coil axis. Furthermore, the skin depth, which is defined as the depth of penetration from the substrate surface where 86% of the Joule heating occurs, is another critical parameter for inductive heating. It depends on the resistivity and the relative magnetic permeability of the heating material, and the applied frequency,[13] and is calculated to be 3.7 μm for nickel at room temperature for this case. The nickel layer thickness of the testing specimen is designed to be comparable to the calculated value for effective inductive heating.

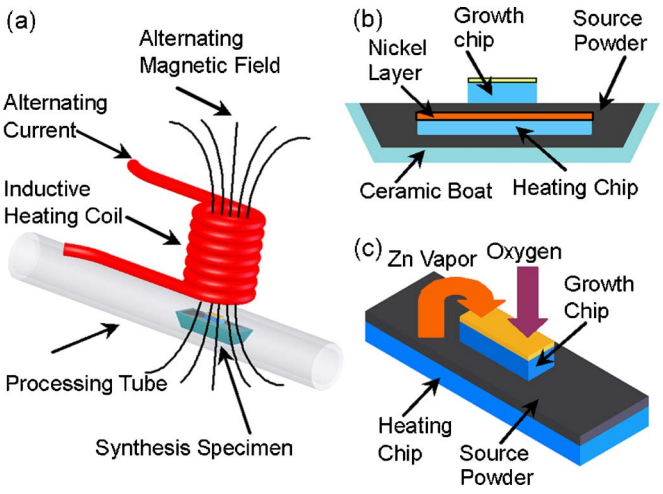

FIG. 1. (Color online) (a) Schematic illustration for ZnO nanowire synthesis setup. (b) Cross sectional view of the synthesis specimen consisting of a heating chip, source powder, and growth chips inside a ceramic boat. (c) Three-dimensional sketch of the heating chip/source powder/growth chips.

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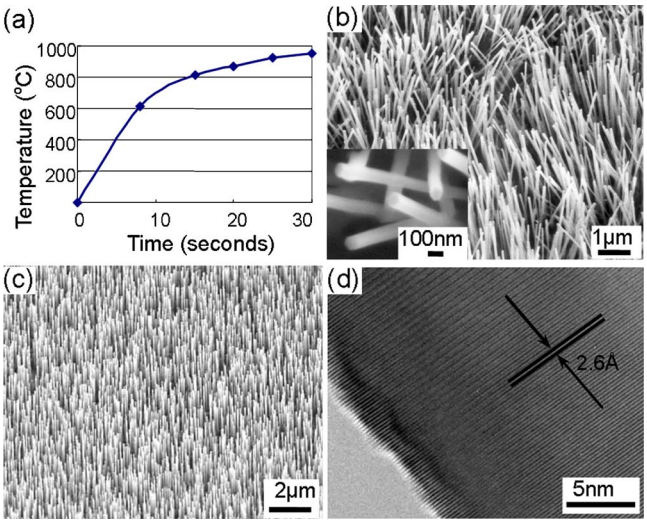

FIG. 2. (Color online) (a) Approximate temperature rise profile for nanowire synthesis at 380 W characterized on the top surface of growth chip at the heating chip center. (b) ZnO nanowires on silicon substrate. Close view image in the inset shows the hexagonal symmetry. (c) Aligned ZnO nanowires synthesized on 4*H*-SiC (0001) substrate. (d) HRTEM image of a single ZnO nanowire showing that the nanowire is highly crystalline and grows along the ⟨0001⟩ direction.

Figure 1(c) is the three-dimensional sketch of the synthesis specimen. The size of the heating chip is 4×8 mm^2, comprised of a lightly doped silicon substrate (p type, ⟨100⟩ orientation, 500-μm-thick, 15 –30 Ω cm) coated with a 3-μm-thick electrodeposited nickel layer. The solid source powder consists of equal weights of ZnO powder (99.99%) and graphite powder (99%). For the growth chip of silicon or 4*H*-SiC (0001), a thin layer of gold (20–30 Å) was deposited on top of the 1×2 mm^2 growth chip as the synthesis catalyst. The preparation of the specimen is as follows. First, a small amount (~0.01–0.02 g) of source powder is added on top of the heating chip inside the ceramic boat and flattened to form a thin layer with an estimated thickness of about 200 μm. The growth chip is placed on top of the thin source powder layer at the heating chip center. Then, the boat is placed inside the processing tube with an argon gas purging of 40 s at 18 SCCM (SCCM denotes cubic centimeter per minute at STP) before experiment. Afterwards, the inductive heating power is turned on with an applied frequency of 11.7 MHz for nanowire synthesis.

Figure 2(a) shows the fast temperature rise profile at the synthesis power of 380 W, which was characterized by temperature indicating paints on the top surface of growth chip. The temperature reaches the synthesis temperature of 900–950 °C within 30 s for the 5 min growth process. Figure 2(b) are the scanning electron microscopy (SEM) images of the resulting ZnO nanowires with diameters ranging from 20 to 120 nm and lengths up to 5 μm grown on silicon substrate. A close SEM view in the inset of Fig. 2(b) illustrates several ZnO nanowires with hexagonal symmetry. Aligned ZnO nanowire growth has also been achieved on the 4*H*-SiC (0001) substrate, as shown in Fig. 2(c). The diameters and lengths of the nanowires were comparable to the nanowires grown on silicon substrates. The strong alignment occurs because of the hexagonal crystal structure, good lattice, and crystal orientation match between the two materials.[14] The crystalline structure of the ZnO nanowires is characterized by using high-resolution transmission electron microscopy (HRTEM) in Fig. 2(d). The distance between the lattice planes is about 2.6 Å, which corresponds to the adjacent (0002) plane distance of ZnO crystal, indicating that the ZnO nanowire is highly crystalline and grows along the ⟨0001⟩ direction. We believe that the catalyst initiated vapor-liquid-solid growth process is applied to the ZnO nanowire synthesis by inductive heating, as no nanowires can grow without gold catalyst deposition in our experiment. Zn vapor is generated from the reduction of ZnO powder by graphite at high temperature, and oxygen is provided from the decomposition of ZnO and the air initially inside the processing tube. At synthesis temperature, gold catalyst absorbs the gaseous reactants to form alloy droplets, which are the preferred sites for ZnO nanowire growth. In addition, it was found that without the argon gas purging before the synthesis process, the high oxygen concentration could result in synthesis of other nanostructures such as nanobelts and nanocombs in addition to nanowires. Similar results were reported in previous investigations using the conventional growth method.[15] Longer purge period led to insufficient supplies of oxygen and the failure of nanowire synthesis.

As the nanowire synthesis process, including the catalyst breakdown, Zn vapor generation, alloy droplet formation from the absorption of reactants in catalyst, and nanowire precipitation is a strong function of temperature; temperature gradient was studied to characterize the ZnO nanowire growth process in the current setup. The synthesis temperatures were calibrated by using temperature indicating paints on the top surface of a group of growth chips, which were then placed on and just outside the heating chip. The temperature is about 900–950 °C in the area within 3 mm distance to the heating chip center and 820–900 °C in the area between 3 and 4 mm away from the center. The temperature drops to about 600 °C at a distance 1 mm away from the edge of the heating chip. As a result, ZnO nanowire length distribution follows the temperature gradient. Figures 3(a) and 3(b) are the synthesis results of ZnO nanowires grown in a 5 min process at the distances of 0.5 and 2.5 mm away from the heating chip center, respectively. ZnO nanowires of ~2–5 μm are found in this area. In Fig. 3(c), ZnO nanowires with shorter lengths of ~0.1–1 μm are found 3.5 mm away from the center, while Fig. 3(d) illustrates that almost no nanowires grow at a position off the heating chip. Figure 3(e) summarizes the length distribution of ZnO nanowires grown at different locations. The reduction of temperature away from the heating chip center results in slower reaction kinetics and reduced Zn vapor supply, leading to shorter nanowire growth. The optimal growth region was found to be within a distance of about 3 mm to the heating chip center in the current setup. Despite the observed thermal gradient, which could be caused by the heat dissipation to the surrounding environment from the heating chip, large-area synthesis with uniform growth might be realized by increasing the inner diameter of the coil and the size of the heating chip. Furthermore, a lower inductive heating power for nanowire synthesis is possible by decreasing the distance between the coil and the synthesis specimen for the presence of stronger magnetic field closer to the coil.

A single ZnO nanowire field-effect transistor (FET) was constructed to characterize the electrical properties of the as-synthesized nanowires. The FET was fabricated on the degenerately doped silicon substrate with a 600-nm-thick SiO_2 layer. An electron beam patterned Ti/Au

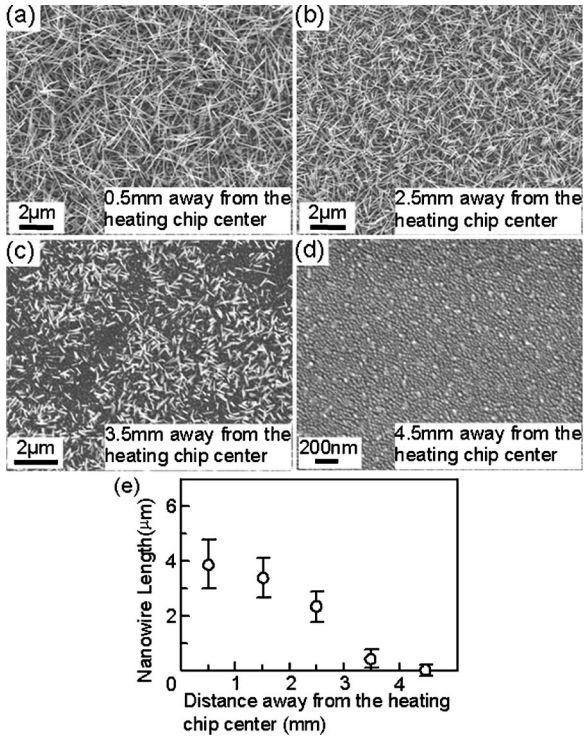

FIG. 3. SEM images correspond to the ZnO nanowire growth results at distances away from the heating chip center of (a) 0.5 mm, (b) 2.5 mm, (c) 3.5 mm, and (d) 4.5 mm. (e) ZnO nanowire length distribution with respect to the growth locations away from the heating chip center. The heating chip center is defined as the origin and is predicted to have the highest temperature.

(50 nm/50 nm) bilayer was evaporated to both ends of an individual nanowire as contact pads. The inset in Fig. 4 is the SEM image of the FET with a channel width of ~60 nm and length of ~1 μm. The current-voltage (I_{sd}-V_{sd}) data of the device are shown in Fig. 4. Higher conductance was obtained by increasing the back gate voltage, indicating *n*-type semiconductor characteristics of the ZnO nanowire possibly due to oxygen vacancies and extra zinc interstitial atoms in the lattice during the synthesis process.[16] An on-off current ratio (I_{on}/I_{off}) of more than 10^4 has been achieved at V_G from −15 to 10 V with V_{sd} of −0.5 V. From the measurements, the mobility μ_e of the channel is calculated to be 6.14 $cm^2/V\,s$ from the relationship[17]

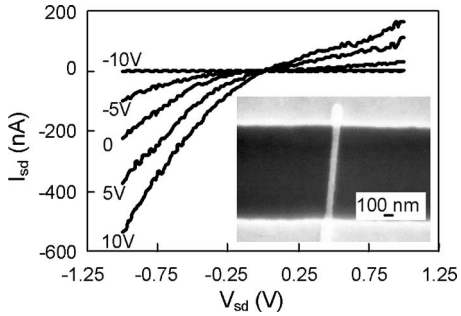

FIG. 4. Current (I_{sd}) vs voltage (V_{sd}) curves recorded at different gate voltages for a single ZnO nanowire FET. The gate voltages are −10, −5, 0, 5, and 10 V, respectively. The inset is the SEM image of the as-fabricated single ZnO nanowire FET.

$$dI_{sd}/dV_G = \mu_e(C/L^2)V_{sd}, \tag{2}$$

where C is the capacitance and L is the channel length. The capacitance is calculated as

$$C = 2\pi\varepsilon\varepsilon_0 L/\ln(2h/r), \tag{3}$$

where $\varepsilon=3.9$ and $h=600$ nm are the dielectric constant and the thickness of the gate oxide layer respectively; r is the nanowire radius. The mobility of the ZnO nanowire is comparable to previously reported ZnO nanowires.[18]

In summary, using a simple and fast inductive heating method, ZnO nanowires have been synthesized in less than 5 min. SEM images show nanowire diameters of 20–120 nm and lengths up to 5 μm. TEM images indicate that the ZnO nanowires are highly crystalline and grow along the ⟨0001⟩ direction. Furthermore, temperature gradient in the current setup was studied to understand the growth process. And the electrical property characterizations of the as-synthesized ZnO nanowires in a FET structure show comparable mobility with ZnO nanowires synthesized by other means. As such, this work presents an alternative way for fast production of ZnO nanowires in a room temperature environment and further illustrates the feasibility of a simple and fast nanoscale synthesis using inductive heating for nanomaterial synthesis.

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