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Direct integration of carbon nanotubes in Si microstructures

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Abstract
In this paper we present a low-cost, room-temperature process for integrating carbon nanotubes on Si microsystems. The process uses localized resistive heating by controlling current through suspended microbridges, to provide local temperatures high enough for CVD growth of carbon nanotubes. Locally grown carbon nanotubes make electrical connections through guidance by electric fields, thus eventually making circuits. The process is scalable to a wafer level batch process. Furthermore, it is controlled electrically, thus enabling automated control. Direct integration of carbon nanotubes in microstructures has great promise for nano-functional devices, such as ultrasensitive chemical sensors. Initial measurements demonstrate the Si–carbon nanotube–Si circuit's potential as a NH_3 sensor.

(Some figures may appear in colour only in the online journal)

1. Introduction

1.1. Carbon nanotubes

Carbon nanotubes (CNTs) have been the *de facto* symbol of nanotechnology ever since their discovery in soot of arc discharge in 1991 by Ijima [1]. CNTs are one of the stable allotropes of carbon. Three-dimensional carbon structures include diamond and graphite; graphene is the 2D structure, CNTs are 1D carbon structures, whereas fullerenes such as C_{60} may be regarded as the 0D carbon structure. CNTs have a highly one-dimensional nature, with diameters in the nm range and lengths in the μm to mm range. Conceptually, a CNT can be regarded as a single graphene sheet rolled up to a cylinder, its *chirality* given by the symmetry along the cylinder periphery. The molecular structure of a CNT is sketched in figure 1.

CNTs exist as single-walled (SWCNT) and multiwalled (MWCNT), the latter consisting of concentrically arranged nanotubes. CNTs have gained massive interest because of their unique properties, such as

- extraordinary mechanical properties: the highest known tensile strength and Young's modulus of any material (besides graphene) [2–6]
- excellent thermal conductivity [7, 8]
- electrical properties depending on chirality: metallic or semiconducting [9, 10]
- high current density capacity [11].

The 1D nature of CNTs makes them ideally suited as model systems for low-dimensional physics. Technologically, they are interesting for a variety of reasons:

- As additives in composites for improving mechanical properties [12, 13]
- As thermal interface materials (TIM) [14]
- As active material in nanoelectronics and nano-electromechanical systems (NEMS) [15, 16].

The latter use is the focus of this paper. The miniaturized nature of CNTs, their high surface-to-volume ratio, their electrical properties and extreme aspect ratios make CNTs a prime candidate for transistors (as CMOS miniaturizing approach a quantum mechanical limit), for ultrasensitive sensors, and for field ionization devices, to mention a few examples.

CNTs are commonly produced by

- arc discharge [1, 17]

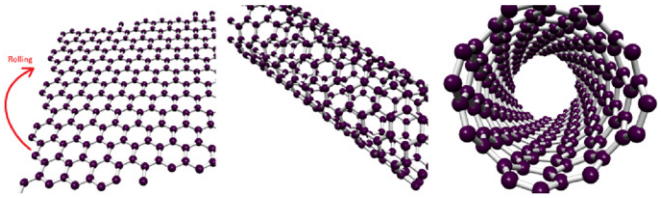

Figure 1. Sketch of single-walled carbon nanotube in different orientations, and the conceptual image of a CNT as a rolled-up graphene sheet.

- chemical vapor deposition (CVD), using a carbon-containing gas [18]
- laser ablation [19].

The similarity in these techniques is that the synthesis temperature of CNTs is high: in the order 800–1000 °C.

1.2. CNT-microsystem integration

Integration of CNTs with microsystems is essential in order to exploit the functionality of CNTs as active material. The microsystem can then act as the bridge connecting the nanomaterial to the macroscopic world. A complete, integrated system should contain MEMS-, CMOS- and CNT-functionality, preferably all integrated on the same die. However, the high synthesis temperature is a major obstacle to CNT-microsystem integration. Processed MEMS/CMOS devices should not be exposed to temperatures above ∼300 °C in the postprocessing. (Somewhat higher temperatures, up to ∼400 °C, may be acceptable if the exposure is very limited in time.)

One way to address this issue is to synthesize CNTs separately, with subsequent assembly to a microsystem. This has indeed been demonstrated, using manual transfer of CNTs by micro-manipulators, and welding the terminals of the CNT to MEMS structures by electron beam-induced deposition (EBID) in a SEM [20]. This is indeed a technique highly relevant in a research laboratory, where the aim is either to measure individual CNT properties or to demonstrate the working principle of an integrated nano-microsystem device. However, it is not scalable to an industrial process because of the serial process occupying high-cost equipment. Other examples of CNT-microsystem integration include CNT wafer-scale growth on a 4″ quartz wafer and a process to transfer CNTs into Si wafer. The transfer process is performed by evaporating 100 nm Au on top of the grown CNTs and using a special tape to transfer the Au layer, including CNTs, from the quartz wafer to the Si wafer to fabricate CNT-FETs by a photolithographic technique [21].

An industrial process for integrating CNTs in microsystems must have

- low cost (CNT integration should not be the dominating system cost)
- batch fabrication possibility
- low process temperature (CMOS compatible below 300 °C)
- localized CNT positions (for integrating active functionality).

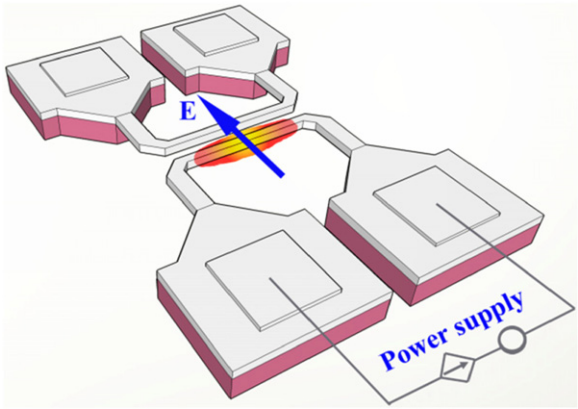

Figure 2. Illustration of the CNT synthesis structure and electrical arrangement.

Such a process would enable postprocessing of CMOS/MEMS-integrated wafers, adding nano-functionality by integrating CNTs. The result would be a truly integrated micro-nano-system at a wafer-level, low-cost process.

This paper describes the efforts toward such a process based on CVD and localized heating. This approach has been addressed by several groups: [22–27]. A review of various local heating methods for this purpose is provided by Sosnowchik *et al* [28]. Resulting CNTs and corresponding circuits are characterized in [29, 30].

2. Experimental details

2.1. Main concept

The main concept of CNT-Si microsystem integration by localized heating was first introduced by Christensen, Englander *et al* [22, 23].

A model microsystem is designed with suspended bridges. This is fabricated using micromachining processes including release of a sacrificial layer such as oxide. The suspended microbridges may consist of single-crystal Si (in a SOI process), or polysilicon (in a process including poly-Si deposition). A catalyst, such as Fe or Ni, is deposited on the bridges. One microbridge is locally heated to reach temperatures sufficient for CVD growth of carbon nanotubes by applying and controlling a current through it. The anchor of the structure itself is kept at ambient temperature. Thermal transport through other channels than conduction through the Si microbridge must be minimized to obtain such a temperature distribution, hence the importance of suspended bridges for avoiding thermal conduction to the substrate. A typical implementation of a growth structure, and the electrical arrangement, is sketched in figure 2, showing a pair of microbridges. One bridge is locally heated to serve as the growth structure. An electric field is established between the two bridges in order to guide the growth direction of CNTs. Figure 3 shows a SEM image of such a growth structure, including wire bonds for electrical connection.

The growth structure is dimensioned to obtain the desired temperature distribution with a reasonable current. Figure 4 shows the simulated temperature distribution of a design, and

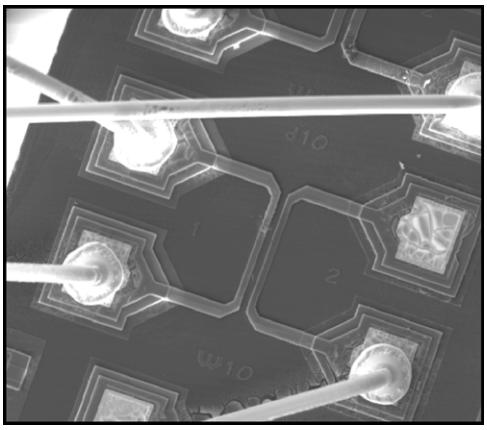

Figure 3. SEM image of a typical microbridge growth structure, with wire bonds as electrical connections.

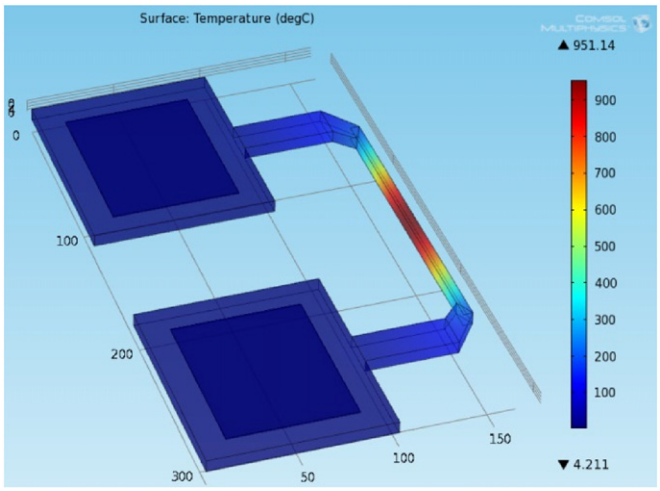

Figure 4. Simulated temperature distribution in a microbridge.

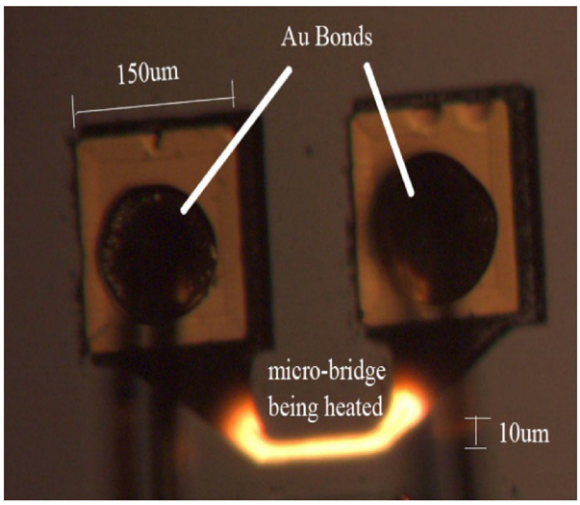

Figure 5. Image of a heated microbridge, showing the localized heating.

figure 5 shows a microscope image of a current-carrying, heated microbridge.

Growth of CNTs occurs when the structure is locally heated in an environment of carbon-containing gas such as acetylene (C_2H_2) or methane (CH_4).

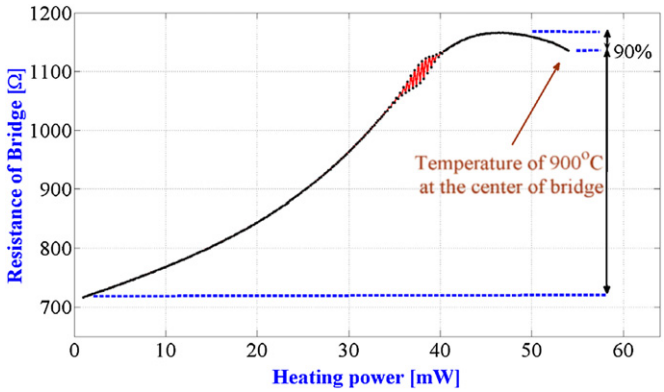

Figure 6. Resistance of Si microbridge, as function of resistive heating power supplied to the bridge. The curve is recorded through a stepwise increase in the heating power. When the resistance is decreased to 90% of the maximum value, the temperature at the center of the microbridge is found to be 900 °C, through calibration with temperature-indicating paint. The oscillating behavior around 35–40 mW is an artifact caused by the time delay in the heating power control, since the measured resistance is an input for this control and the TCR is large. Details of this temperature control are found in [27].

2.2. Present experiment

The microstructure used in the present experiment consists of two suspended polysilicon microbridges, 5 μm wide and 160 μm long. The two microbridges are separated by 15 μm, and they are suspended 3.5 μm above the substrate (after etching of a sacrificial layer of this thickness). A double thin layer of 3 nm thick Fe and 2 nm thick Ni is evaporated to serve as the catalyst. No patterning of the catalyst was needed, since the selection of areas for CNT growth is performed by the localized resistive heating. Only the center area of the microbridge will reach the required temperature (as indicated in figure 4), so CNTs are expected only in this area. The synthesis is accomplished using resistive heating on the growth structure while a local electric field is established between the two bridges to guide the growth direction of CNTs [1, 20]. The synthesis is conducted in a room-temperature chamber with an acetylene (C_2H_2) gas flow of 30 ccm (cubic centimeter per minute) at a pressure of 0.4 bar after local heating to the desired temperature (850–950 °C). Acetylene (C_2H_2) gas is known to allow CNT CVD growth at somewhat lower temperatures than other carbon-containing gases [26], hence this gas is a natural choice as the carbon source for the present experiment.

The temperature at the center of the microbridge is monitored by measuring the resistance of the microbridge, as shown in figure 6. Doped Si shows a highly temperature-sensitive resistivity, with a positive temperature coefficient of resistivity (TCR) at moderate temperatures, and a negative TCR at higher temperatures when intrinsic conductivity becomes dominating. The temperature, and hence the local resistivity, will vary along the length of the microbridge. The measured resistance of the microbridge will thus arise from a sum of contributions with different temperature and resistivity. The temperature-to-resistance relation is calibrated through the use of temperature-sensitive indicating paint. It is found that a temperature of 900 °C (maximum temperature along

the length of the microbridge) is obtained in the negative-TCR part of the resistance versus heating power curve, more specifically when the resistance is 90% of the maximum value (cf figure 6). The resistance versus heating power curve of figure 6 is in accordance with calculations based on the temperature profile in figure 4, and finite-element modeling of the microbridge using the temperature-dependent resistivity of doped Si. Details of this calculation are found in [27]. This criterion for detecting a maximum temperature of 900 °C is found to be valid for a variety of microbridge geometries, for polysilicon as well as single crystal silicon (SOI), and also for a variety of gas pressures and flow rates. The resistance value at this stage is $R \sim 1.5R_T$, R_T being the room temperature resistance [27].

When CNTs grow to connect the two microbridges, it can be detected electrically, either by monitoring the electrical potential of the second microbridge, or by monitoring the current across the microbridges (through the CNTs).

The described method of direct integration of CNTs in Si microstructures uses only electrical parameters for the control, stabilization and measurement of the growth temperature. Also, electrical measurements are used to control the number of CNT connections made in every single circuit. There is no need for additional equipment for temperature control, such as optical or spectroscopic equipment. Electrical control enables parallel processing, can be automated, and is readily implemented in an industrial setting. The method of pure electrical control thus demonstrates the possibility for a CNT-to Si integration process to be compatible with wafer-level manufacturing.

2.3. NH_3 sensitivity demonstration

CNTs integrated in Si microsystems have been demonstrated to function as gas sensors [31]. Until now, this has not been verified on systems made by the described technique using purely electrical control.

In order to demonstrate the possibility for such a Si–CNT–Si circuit to function as a gas sensor, the following experiment was carried out:

The chip with the Si–CNT–Si circuit, manufactured as described above (section 2.2), was put in a chamber, which was then evacuated. A bias voltage of 0.1 V was applied between the two microbridges connected by CNTs. The resistance of the circuit was monitored by measuring the current through the CNTs under this constant bias voltage. A given amount of NH_3 was injected in the chamber, and the resistance change was monitored as a function of time. After NH_3 exposure, the chamber was evacuated prior to a new, higher concentration NH_3 exposure.

The effective NH_3 concentration in the chamber was found from the volume of NH_3 gas injected into the chamber. This volume was extracted by a syringe from a closed flask containing NH_3 gas over a NH_3/ethanol solution.

3. Results and discussion

Individual CNT connections were detected by monitoring the current across the two bridges as a function of synthesis time, as shown in figure 7. Figure 7 shows the first CNT connection being made 68.8 s after the introduction of C_2H_2 in the chamber, while the second CNT connection is established 1.3 s later. As can be deduced from the different magnitudes of the current jumps, the two CNT connections have different resistance: The first corresponds to 270 kΩ (37 μA current jump at 10 V), and the second corresponds to 170 kΩ (58 μA current jump at 10 V).

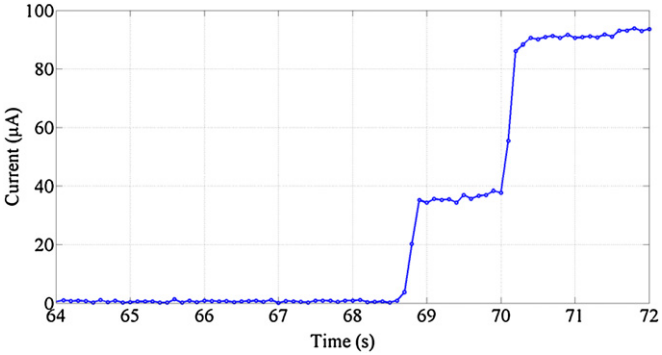

Figure 7. Current across bridges versus synthesis time. Each jump signifies a new CNT connection established. The voltage over the Si–CNT–Si circuit is 10 V.

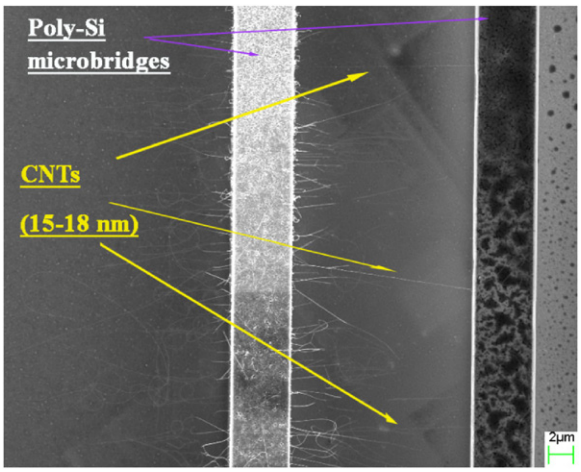

Figure 8. A close-up SEM image of locally synthesized CNTs, where some connect two polysilicon microstructures.

Figure 8 shows a scanning electron microscopy (SEM) image of locally synthesized CNTs, some connecting the two microbridges. The CNTs connect the bridges over a gap of 15 μm. It is worth noting that the CNTs are very straight, even with relatively moderate electric fields (around 0.2 V μm^{-1}). There are CNTs growing also in the opposite direction, probably due to the fringing electric field.

SEM inspection shows that the synthesized CNTs have a good uniformity, high aspect ratios up to 1000:1 (length/diameter), and an apparently narrow distribution of the diameters, with many in the range of 15–18 nm. A closer inspection reveals that more than half the CNTs have diameters in the range of 13–18 nm [27].

Current I–voltage V measurement is taken between the two microbridges, the connection being made by three CNTs in parallel. The I–V curve in figure 9 shows a fairly ohmic behavior in the voltage range −1 V to +1 V, and an overall

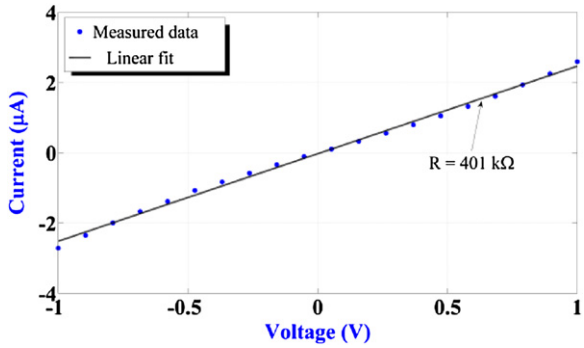

Figure 9. *I–V* curve of three bridging CNTs (in parallel), measured between two microbridges, at room temperature.

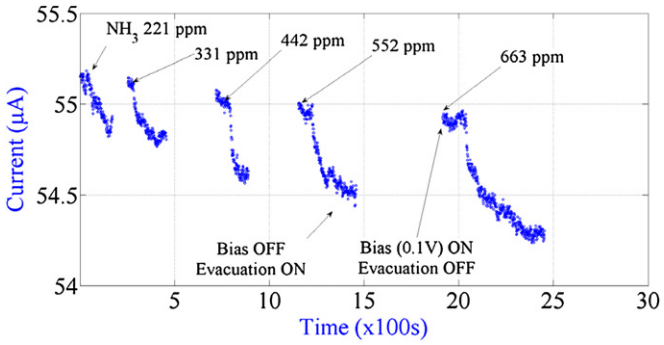

Figure 10. Resistance in a Si–CNT–Si circuit upon exposure to controlled NH_3 atmosphere. Resistance is monitored by current measurements at constant voltage bias.

resistance of 400 kΩ. The present result is comparable with the previous results from [22, 32] (from 400 kΩ to 6 MΩ). Data for larger voltage values were not recorded, as this has been found to easily damage the CNT connections.

The measured resistance consists both of the intrinsic resistance of the carbon nanotube, and of the contact resistance at the CNT–Si interface. The current data are insufficient to quantitatively determine those values individually. Measurements of resistance of individual CNTs in the literature [33] indicate a resistance of ∼30 kΩ for CNTs with comparable diameter, but shorter length, than ours. Previously published estimates of the relation between the contact resistance and the intrinsic resistance of CNTs in a system comparable to ours indicate that the two are of the same order of magnitude [29]. Many techniques to reduce the contact resistance have been studied. Chiamori *et al* demonstrated a simple and fast annealing technique for locally synthesized CNTs that can decrease the resistance by a factor ranging from 20% to over 80% [32].

The resistance in the presence of a controlled NH_3 atmosphere is shown in figure 10. The measured current decreases upon exposure to NH_3, signifying an increased resistance in the circuit. The effect clearly increases with increasing NH_3 concentration. The present measurements thus demonstrate the direct integration of CNTs in Si microsystems as a potential method for making a nanomaterial-based NH_3 sensor. The experiments are, however, at an initial state. Sensitivity, stability and linearity are expected to be greatly improved as the process is more fully characterized and optimized in ongoing work.

4. Conclusion

The process shown for direct integration of CNTs in Si microsystems is demonstrated to obtain nanotubes that can close the circuit between two defined microstructures. For a suitable microsystem design, the process is therefore capable of producing functional nano-devices in a single process step.

The process is CMOS compatible and low cost. A crucial process parameter is the local temperature, governed by the current flowing in the microbridge. Since the temperature can be measured through a resistance measurement, it can be controlled automatically. Since individual CNT connections can be measured electrically, an automated process may be set up to produce the desired number of CNT connections. This ensures that the process can be scaled to an effective, easily controlled, wafer-level batch process.

Potentially, the process may be used as a last process step for integrated CMOS + MEMS wafers, producing truly integrated micro-nano-systems. The ability for such a system to work as a gas sensor is demonstrated through showing a model system's sensitivity to NH_3.

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